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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/059,898  | 01/28/2002  | Oleg Siniaguine      | M-4532-8P US        | 8562             |
| 32605   | 7590        | 11/18/2003           | EXAMINER            |                  |
| MACPHERSON KWOK CHEN & HEID LLP<br>1762 TECHNOLOGY DRIVE, SUITE 226<br>SAN JOSE, CA 95110 |             |                      | VU, HUNG K          |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2811                |                  |

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/059,898

Applicant(s)

SINIAGUINE, OLEG

Examiner

Hung K. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2 and 8-10 is/are allowed.
- 6) ☒ Claim(s) 3-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 3 is objected to because of the following informalities:

In claim 3, line 1, "The" should be changed to "A" for clarity

In claim 3, line 16, "out" should be changed to "outer" for clarity.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Youmans (PN 3,761,782, of record).

Youmans disclose, as shown in Figures 10-11, an integrated circuit structure in combination with a first substrate, wherein the integrated circuit structure comprises:

a body comprising a semiconductor substrate (11,12) which has a top surface and a bottom surface, wherein one or more through holes (21) pass through the substrate between the top and bottom surfaces, the body comprising one or more circuit elements formed in and/or over the top surface of the semiconductor substrate;

a conductor (41) formed in each through hole and protruding from the bottom surface of the semiconductor substrate, the conductor in each through hole being coupled to one or more of the circuit elements;

a dielectric (18) separating the conductor in each through hole from the semiconductor substrate, wherein at each through hole the dielectric forms a protrusion on the bottom of the body around the conductor;

wherein at each through hole the conductor protrudes from the dielectric on the bottom of the body, the conductor thus having a protruding outer surface not covered by the dielectric, wherein at least a portion of the protruding outer surface extends downward and faces laterally away from the through hole, and the portion of the protruding outer surface is either vertical or sloped outwards (laterally away from the through hole) when the surface is traced down;

wherein the protruding outer surface of each conductor is attached to the first substrate with a bonding material (42) provide a conductive bond between the conductor and the first substrate, wherein the bonding material reaches and at least partially covers the portion of the protruding outer surface which is either vertical or sloped outwards [Figures 10 and 11].

With regard to claims 4, Youmans discloses the bonding material comprises solder which bonds the conductor to the first substrate, wherein the solder reaches and at least partially covers the portion of the protruding outer surface portion which either vertical of slop outwards [Figures 10 and 11].

3. Claims 3-4 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Gnadinger (PN 5,229,647, of record).

Gnadinger disclose, as shown in Figures 4 and 5, an integrated circuit structure in combination with a first substrate, wherein the integrated circuit structure comprises:

a body (10) comprising a semiconductor substrate which has a top surface and a bottom surface, wherein one or more through holes (21) pass through the substrate between the top and bottom surfaces, the body comprising one or more circuit elements formed in and/or over the top surface of the semiconductor substrate;

a conductor (28,20) formed in each through hole and protruding from the bottom surface of the semiconductor substrate, the conductor in each through hole being coupled to one or more of the circuit elements;

a dielectric (24) separating the conductor in each through hole from the semiconductor substrate, wherein at each through hole the dielectric forms a protrusion on the bottom of the body around the conductor;

wherein at each through hole the conductor protrudes from the dielectric on the bottom of the body, the conductor thus having a protruding outer surface not covered by the dielectric, wherein at least a portion of the protruding outer surface extends downward and faces laterally away from the through hole, and the portion of the protruding outer surface is either vertical or sloped outwards (laterally away from the through hole) when the surface is traced down;

wherein the protruding outer surface of each conductor is attached to the first substrate with a bonding material (20) provide a conductive bond between the conductor and the first

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substrate, wherein the bonding material reaches and at least partially covers the portion of the protruding outer surface which is either vertical or sloped outwards [Figures 4 and 5].

With regard to claims 4, Gnadinger discloses the bonding material comprises solder which bonds the conductor to the first substrate, wherein the solder reaches and at least partially covers the portion of the protruding outer surface portion which either vertical of slop outwards [Figures 4 and 5].

With regard to claims 6, Gnadinger discloses the conductor comprises a first conductive layer (20) and a second conductive layer (28) separating the first conductive layer from the dielectric; wherein the second conductive layer is not present o the protruding outer surface [Figure 4].

With regard to claims 7, Gnadinger discloses the first conductive layer is solder wettable, and the second conductive layer is not solder wettable [Col. 3, line 58 – Col. 4, line 36].

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Youmans (PN 3,761,782, of record) in view of Baba et al. (PN 5,969,426, of record).

Youmans discloses the claimed invention including the integrated circuit structure as recited in the rejection above. Youmans does not disclose the bonding material fills the entire space between the integrated circuit structure and the first substrate. However, Baba et al. discloses a bonding material (41) fills the entire space between the integrated circuit structure (31) and the first substrate (34). Note Figures 21d and 22d of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Youmans having bonding material fills the entire space between the integrated circuit structure and the first substrate, such as taught by Baba et al. in order to provide additionally mechanical support.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger (PN 5,229,647, of record) in view of Baba et al. (PN 5,969,426, of record).

Gnadinger discloses the claimed invention including the integrated circuit structure as recited in the rejection above. Gnadinger does not disclose the bonding material fills the entire space between the integrated circuit structure and the first substrate. However, Baba et al. discloses a bonding material (41) fills the entire space between the integrated circuit structure (31) and the first substrate (34). Note Figures 21d and 22d of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Gnadinger having bonding material fills the entire space between the integrated

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circuit structure and the first substrate, such as taught by Baba et al. in order to provide additionally mechanical support.

*Allowable Subject Matter*

6. Claims 3 and 8-10 are allowed.

*Response to Arguments*

7. Applicant's arguments filed 09/03/03 have been fully considered but they are not persuasive.

It is argued, at page 8 of the Remarks, that Figure 10 of Youmans does not disclose the bonding material 42 reaches or at least partially covers that portion of the surface of conductor 41 which extends downward and faces laterally away from hole 21. This argument is not convincing because Youmans discloses the bonding material 42 reaches or at least partially covers a side portion of portion of the surface of conductor 41 which extends downward and faces laterally away from hole 21. Further, in Figure 11, Youmans also discloses the bonding material 58 reaches or at least partially covers a side portion of portion of the surface of conductor 41 which extends downward and faces laterally away from hole 21. Therefore, Applicant's claim 3 does not distinguish over the Youmans reference.

It is argued, at page 8 of the Remarks, that Gnadinger teaches away from a bonding material because Gnadinger teaches away from forming a mechanical bonding between the two wafers.

This argument is not convincing because the feature upon which applicant relies (i.e., mechanical



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bonding between the two wafers) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Also note that Gnadinger teaches not to form a "rigid mechanical bond" between wafers 10 does not necessary mean there is no bonding. In fact, there is still a bond between the wafers 10, although, it is not a "rigid bond". Therefore, Applicant's claim 3 does not distinguish over the Gnadinger reference.

It is argued, at page 9 of the Remarks, that Baba et al. does not teach the material 41 provides a conductive bond as recited in claim 3. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In fact, Baba et al. teaches the bonding material fills the entire space between the integrated circuit structure and the first substrate to provide additionally mechanical support

### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

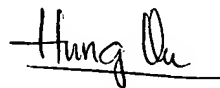
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

November 14, 2003

A handwritten signature in black ink, appearing to read "Hung Vu", written over a horizontal line.

Hung Vu

Patent Examiner